IN THE CLAIMS

1. (Original) A method for manufacturing a gate spacer for self-aligned contacts comprising:

forming a gate stack on a semiconductor substrate;

forming a conformal dielectric layer over the gate stack;

applying an etch-stop material layer over the conformal dielectric layer;

removing an upper portion of the etch-stop material layer to expose an upper portion of the conformal dielectric layer;

etching back the exposed conformal dielectric layer;

removing the remaining etch-stop material layer; and

etching back the etched-back conformal dielectric layer to form a gate spacer.

2. (Original) The method of claim 1, wherein the gate stack comprises a gate dielectric, a gate electrode, a hard mask, and a patterned oxide layer.

3. (Original) The method of claim 2, wherein a top surface of the gate spacer is substantially lower than that of the hard mask.

4. (Original) The method of claim 1, wherein a top portion of the gate spacer is approximately 400 Å higher than that of the gate electrode.

5. (Original) The method of claim 1, wherein the etch-stop material layer comprises an organic material.

6. (Original) The method of claim 5, wherein the etch-stop material layer is a photoresist layer.

7. (Original) The method of claim 6, wherein removing the photoresist layer comprises etching the photoresist layer using a gas mixture of SF6, CF4, O2 and HBr.

8. (Original) The method of claim 1, wherein the etch-stop material layer is used as an etch stopper during etching of the exposed conformal dielectric layer.

9. (Original) The method of claim 1, wherein a thickness of the etch-stop material layer is more than approximately 1000 Å.

10. (Currently Amended) A method for manufacturing a semiconductor device comprising:

forming a gate stack on a semiconductor substrate;

forming a gate spacer on sidewalls of the gate stack, wherein the gate spacer includes a top portion substantially lower than a top of the gate stack;

forming a blanket etching stop layer over the gate stack and semiconductor substrate; and

forming an interlayer insulating layer over the gate stack including the gate spacer.

11. (Cancelled)

12. (Cancelled)

13. (Currently Amended) The method of claim ~~11~~10, further comprising forming a self-aligned contact hole within the interlayer insulating layer adjacent the gate stack.

14. (Original) A method of claim 13, further comprising:

depositing a conductive material within the contact hole; and

planarizing the conductive material to form a contact pad.